

PTO/SB/21 (09-04)

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**TRANSMITTAL
FORM**

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Total Number of Pages in This Submission 18

Application Number	10/815,453
Filing Date	March 31, 2004
First Named Inventor	Ricardo E. Gonzalez
Art Unit	2142
Examiner Name	Andrew T. Caldwell
Attorney Docket Number	PA2718US

ENCLOSURES (Check all that apply)

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|---|--|--|
| <input type="checkbox"/> Fee Transmittal Form
<input type="checkbox"/> Fee Attached
<input type="checkbox"/> Amendment/Reply
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below):
1) Confirmation postcard;
2) Duplicate of IDS;
3) PTO/SB/08 (6 pp., x2);
4) Copies of 22 cited nonpatent references;
5) List of co-pending applications. |
|---|--|--|

Remarks

Total page number does not include postcard or nonpatent references.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Carr & Ferrell LLP	Cust. No. 22830
Signature	<i>Peter L. Holland</i>	
Printed name	Peter L. Holland	
Date	June 6, 2007	Reg. No. 57,113

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Typed or printed name	Peter L. Holland, Reg. No. 57,113	Date	June 6, 2007

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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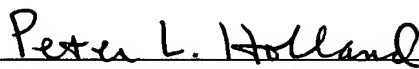


IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Ricardo E. Gonzalez et al.
APPLICATION NO.: 10/815,453
FILED: March 31, 2004
TITLE: Configuring a Multi-Processor System
EXAMINER: Andrew T. Caldwell
GROUP ART UNIT: 2142
ATTY.DKT.NO.: PA2718US

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 6, 2007.


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INFORMATION DISCLOSURE STATEMENT
Under 37 C.F.R. §§ 1.56, and 1.97-1.98

SIR:

Pursuant to the provisions of 37 C.F.R. §§ 1.56 and 1.97-98 of the Rules of Practice in Patent Cases, enclosed herewith is form PTO-SB-08, listing several references, and a list of Co-Pending Applications.

The Examiner is requested to make these references of official record in the application. The references cited may be material to examination of the application and are submitted in compliance with Applicant's duty of disclosure as defined by 37 C.F.R. § 1.56. No representation is made or intended as to the completeness of this list, nor is the inclusion of any reference on this list an admission that it is prior art or pertinent to this application.

Applicant believes no fee is due with this submission. If a fee is due, however, the Commissioner is hereby authorized to charge any necessary fee to Account Number 06-0600. A copy of this statement is submitted in duplicate for this purpose.

Respectfully submitted,
Ricardo E. Gonzalez et al.

June 6, 2007

By:



Peter L. Holland, Reg. No. 57,113

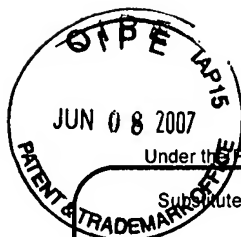
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 6

Complete if Known

Application Number	10/815,453
Filing Date	March 31, 2004
First Named Inventor	Ricardo E. Gonzalez
Art Unit	2142
Examiner Name	Andrew T. Caldwell
Attorney Docket Number	PA2718US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 6,698,015 B1	02-24-2004	Moberg et al.	
		US- 6,799,236 B1	09-28-2004	Dice et al.	
		US- 5,822,588	10-13-1998	Sterling et al.	
		US- 6,817,013 B2	11-09-2004	Tabata et al.	
		US- 6,968,544 B1	11-22-2005	Schneider	
		US- 7,178,062 B1	02-13-2007	Dice	
		US- 5,999,734	12-07-1999	Willis et al.	
		US- 6,622,233 B1	09-16-2003	Gilson	
		US- 5,535,406	07-09-1996	Kolchinsky	
		US- 6,092,174	07-18-2000	Roussakov	
		US- 5,956,518	09-21-1999	DeHon et al.	
		US- 2004/0019765 A1	01-29-2004	Klein, Jr.	
		US- 5,361,373	11-01-1994	Gilson	
		US- 2005/0166038 A1	07-28-2005	Wang et al.	
		US- 5,488,612	01-30-1996	Heybruck	
		US- 5,258,668	11-02-1993	Cliff et al.	
		US- 5,260,610	11-09-1993	Pedersen et al.	
		US- 5,260,611	11-09-1993	Cliff et al.	
		US- 5,274,581	12-28-1993	Cliff et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		EP 0 668 659 A2	08-23-1995	Pilkington Germany		
		EP 0 507 507 A2	10-07-1992	American Telephone		
		TW 152,994	07-22-2002	Adaptive Silicon, Inc.		
		TW 168,210	04-15-2003	Adaptive Silicon, Inc.		
		TW 152,355	07-10-2002	Adaptive Silicon, Inc.		

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STATEMENT BY APPLICANT**

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Application Number	10/815,453
Filing Date	March 31, 2004
First Named Inventor	Ricardo E. Gonzalez
Art Unit	2142
Examiner Name	Andrew T. Caldwell
Attorney Docket Number	PA2718US

Sheet **2** of **6****U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,343,406	08-30-1994	Freeman et al.	
		US- 5,414,377	05-09-1995	Freidin	
		US- 5,726,584	03-10-1998	Freidin	
		US- 5,426,378	06-20-1995	Ong	
		US- 5,920,202	07-06-1999	Young et al.	
		US- 5,926,036	07-20-1999	Cliff et al.	
		US- 5,963,050	10-05-1999	Young et al.	
		US- 5,977,793	11-02-1999	Reddy et al.	
		US- 5,982,195	11-09-1999	Cliff et al.	
		US- 5,986,465	11-16-1999	Mendel	
		US- 2001/0049816	12-06-2001	Rupp	
		US- 6,633,181 B1	10-14-2003	Rupp	
		US- 5,357,152	10-18-1994	Jennings, III et al.	
		US- 5,742,180	04-21-1998	DeHon et al.	
		US- 5,436,574	07-25-1995	Veenstra	
		US- 4,635,261	01-06-1987	Anderson et al.	
		US- 4,766,659	08-30-1988	Cronenwett et al.	
		US- 4,893,311	01-09-1990	Hunter et al.	
		US- 6,353,841 B1	03-05-2002	Marshall et al.	

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Sheet 3 of 6

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		Number-Kind Code ² (if known)			
		US- 6,237,079 B1	05-22-2001	Stoney	
		US- 5,488,612	01-30-1996	Heybruck	
		US- 5,847,578	12-08-1998	Noakes et al.	
		US- 6,415,424 B1	07-02-2002	Arimilli et al.	
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		US- 5,682,493	10-28-1997	Yung et al.	
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		US- 5,652,875	07-29-1997	Taylor	
		US- 5,696,956	12-09-1997	Razdan et al.	
		US- 5,784,636	07-21-1998	Rupp	
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		US- 6,732,354 B2	05-04-2004	Ebeling et al.	
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		US- 2003/0108119 A1	06-12-2003	Mohebbi et al.	
		US- 6,721,884 B1	04-13-2004	De Oliveira Kastrup Pereira et al.	
		US- 6,426,648 B1	07-30-2002	Rupp	
		US- 7,062,520 B2	06-13-2006	Rupp	
		US- 6,857,110 B1	02-15-2005	Rupp et al.	
		US- 6,744,274 B1	06-01-2004	Arnold et al.	

FOREIGN PATENT DOCUMENTS

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Sheet	4	of	6
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Examiner Name	Andrew T. Caldwell
Attorney Docket Number	PA2718US

Sheet 5

of

6

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BEECK et al., "CRISP: A Template for Reconfigurable Instruction Set Processors," FPL 2001, LNCS 2147, pp. 296-305, Springer-Verlag Berlin Heidelberg, 2001.	
		BECHADE et al., "Programmable Arithmetic/Logic Circuits," IBM Technical Disclosure Bulletin, U. S. IBM Corp., New York, Vol. 3, No. 11, April 1981, pp. 4870-4873, XP-000713711.	
		DEHON, ANDRE, "Transit Note #118 Notes on Coupling Processors with Reconfigurable Logic," M.I.T. Transit Project, Last Updated March 21, 1995.	
		TANENBAUM, ANDREW S., "Modern Operating Systems," 2001, 2nd edition, Prentice Hall, New Jersey, p. 31.	
		HENNESSY, JOHN L. and DAVID A. PATTERSON, "Computer Organization and Design: The Hardware/Software Interface," 1998, 2nd edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA, p. 345.	
		LEE, K.C., "A Virtual Bus Architecture for Dynamic Parallel Processing," February 1993, IEEE Transactions on Parallel and Distributed Systems, Vol. 4, No. 2, pp. 121-130.	
		GOLDBLATT, KIM, "The Low-Cost, Efficient Serial Configuration of Spartan FPGAs," November 13, 1998, XAPP098 (Version 1.0), XILINX.	
		SCOTT, STEVEN L. and GREGORY M. THORSON, "The Cray T3E Network: Adaptive Routing in a High Performance 3D Torus," August 15-16, 1996, HOT Interconnects IV, Stanford University.	
		GOLESTANI, S. JAMALODDIN, "A Stop-and-Go Queuing Framework for Congestion Management," 1990, Proc. of the ACM Symposium on Communications Architectures & Protocols, ACM Press, New York, NY, pp. 8-18.	
		DALLY, WILLIAM J. and CHARLES L. SEITZ, "Deadlock Free Message Routing in Multiprocessor Interconnection Networks," May 10, 1985, Computer Science Department, California Institute of Technology.	

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Sheet	6	of	6	Attorney Docket Number	PA2718US

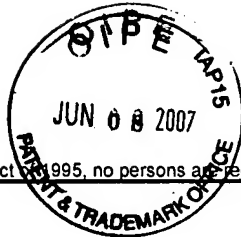
NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
		GARLAN, DAVID and MARY SHAW, "An Introduction to Software Architecture," January 1994, CMU-CS-94-166, School of Computer Science, Carnegie Mellon University, Pittsburgh, PA.		
		INTEL and HEWLETT-PACKARD, "IA-64 Application Instruction Set Architecture Guide," Revision 1.0, 1999, pp. C-1 through C.		
		HWANG, KAI, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," 1993, McGraw Hill, pp. 182-183.		
		YE, Z.A. et al., "CHIMAERA: a high-performance architecture with a tightly-coupled reconfigurable functional unit," June 10-14, 2000, Proc. of the 27th International Symposium on Computer Architecture, pp. 225-235.		
		MIPS Technologies, Inc., "MIPS Extension for Digital Media with 3D," 1996, pp. 1-26.		
		BORGATTI, MICHELE et al., "A Reconfigurable System featuring Dynamically Extensible Embedded Microprocessor, FPGA and Customisable I/O," 2002, IEEE Custom Integrated Circuits Conference, pp. 1-4.		
		RAZDAN, RAHUL and MICHAEL D. SMITH, "A High-Performance Microarchitecture with Hardware-Programmable Functional Units," November 1994, Proc. of MICRO-27, pp. 1-9.		

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Sheet 1 of 6

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Application Number	10/815,453
Filing Date	March 31, 2004
First Named Inventor	Ricardo E. Gonzalez
Art Unit	2142
Examiner Name	Andrew T. Caldwell
Attorney Docket Number	PA2718US

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 6,698,015 B1	02-24-2004	Moberg et al.	
		US- 6,799,236 B1	09-28-2004	Dice et al.	
		US- 5,822,588	10-13-1998	Sterling et al.	
		US- 6,817,013 B2	11-09-2004	Tabata et al.	
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		US- 5,260,610	11-09-1993	Pedersen et al.	
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		US- 5,274,581	12-28-1993	Cliff et al.	

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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
		EP 0 668 659 A2	08-23-1995	Pilkington Germany		
		EP 0 507 507 A2	10-07-1992	American Telephone		
		TW 152,994	07-22-2002	Adaptive Silicon, Inc.		
		TW 168,210	04-15-2003	Adaptive Silicon, Inc.		
		TW 152,355	07-10-2002	Adaptive Silicon, Inc.		

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Attorney Docket Number	PA2718US

Sheet **2** of **6****U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,343,406	08-30-1994	Freeman et al.	
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		US- 5,920,202	07-06-1999	Young et al.	
		US- 5,926,036	07-20-1999	Cliff et al.	
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		US- 5,357,152	10-18-1994	Jennings, III et al.	
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		US- 6,237,079 B1	05-22-2001	Stoney	
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		Number-Kind Code ² (if known)			
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		BEECK et al., "CRISP: A Template for Reconfigurable Instruction Set Processors," FPL 2001, LNCS 2147, pp. 296-305, Springer-Verlag Berlin Heidelberg, 2001.	
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		DALLY, WILLIAM J. and CHARLES L. SEITZ, "Deadlock Free Message Routing in Multiprocessor Interconnection Networks," May 10, 1985, Computer Science Department, California Institute of Technology.	

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Sheet 6 of 6

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		GARLAN, DAVID and MARY SHAW, "An Introduction to Software Architecture," January 1994, CMU-CS-94-166, School of Computer Science, Carnegie Mellon University, Pittsburgh, PA.	
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**IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANT(S): Ricardo E. Gonzalez et al.

APPLICATION NO.: 10/815,453

FILED: March 31, 2004

TITLE: Configuring a Multi-Processor System

EXAMINER: Andrew T. Caldwell

GROUP ART UNIT: 2142

ATTY.DKT.NO.: PA2718US

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P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

**List of Co-Pending Patents or Patent Applications That May Be Directed
Towards Similar Subject Matter**

Examiner's Initials	Application Number	First-Named Inventor	Title	Filing Date
	10/630,542	Kenneth Williams	Defining Instruction Extensions in a Standard Programming Language	07-29-2003
	10/404,706	Scott D. Johnson	Extension Adapter	03-31-2003
	10/394,824	Charle' Rupp	Transitive Processing Unit for Performing Complex Operations	03-21-2003
	10/686,882	Kenneth Williams	Instruction Set for Efficient Bit Stream and Byte Stream I/O	10-15-2003
	10/750,714	Ricardo Gonzalez	Systems and Methods for Software Extensible Multi-Processing	12-31-2003
	10/815,453	Ricardo Gonzalez	Configuring a Multi-Processor System	03-31-2004
	11/021,247	Ricardo Gonzalez	Systems and Methods for Selecting I/O Interfaces for Configurable Processors	12-21-2004
	11/129,146	Ricardo Gonzalez	Long Instruction Word Processing with Instruction Extensions	05-12-2005
	11/099,280	Jeffrey M. Arnold	Video Processing System with Reconfigurable Instructions	04-04-2005
	11/204,555	Jeffrey M. Arnold	Programmable Logic Configuration for Instruction Extensions	08-15-2005
Examiner's Signature:				Date